EXHIBIT 17

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CONTROL NO.	FILING DATE	PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
95000100	6/28/05	6725356	

EXAMINER
Richard Ellis

ART UNIT	PAPER
2183	

Leonard Guzman, c/o Michael Fogarty, ESQ.
MCDERMOTT WILL & EMERY
600 13th St. N.W.
Washington, D.C. 20005-3096

DATE MAILED:

5/3/06

INTER PARTES REEXAMINATION COMMUNICATION

BELOW/ATTACHED YOU WILL FIND A COMMUNICATION FROM THE UNITED STATES PATENT AND TRADEMARK OFFICE OFFICIAL(S) IN CHARGE OF THE PRESENT REEXAMINATION PROCEEDING.

All correspondence relating to this *inter partes* reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this communication.

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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

David L. McCombs
Hanyes & Boone, LLP
901 Main St. Suite 3100
Dallas, TX. 75202

Transmittal of Communication to Third Party Requester *Inter Partes* Reexamination

REEXAMINATION CONTROL NUMBER *95/000,100*.

PATENT NUMBER *6,725,356*.

TECHNOLOGY CENTER *2100*.

ART UNIT *2183*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above-identified reexamination proceeding. 37 CFR 1.903.

Prior to the filing of a Notice of Appeal, each time the patent owner responds to this communication, the third party requester of the *inter partes* reexamination may once file written comments within a period of 30 days from the date of service of the patent owner's response. This 30-day time period is statutory (35 U.S.C. 314(b)(2)), and, as such, it cannot be extended. See also 37 CFR 1.947.

If an *ex parte* reexamination has been merged with the *inter partes* reexamination, no responsive submission by any *ex parte* third party requester is permitted.

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of the communication enclosed with this transmittal.

OFFICE ACTION IN INTER PARTES REEXAMINATION	Control No.	Patent Under Reexamination	
	95/000,100	6725356	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address. --

Responsive to the communication(s) filed by:
Patent Owner on 11/28/2005, 12/8/2005, and 3/2/2006.
Third Party(ies) on No response filed.

RESPONSE TIMES ARE SET TO EXPIRE AS FOLLOWS:

For Patent Owner's Response:
2 MONTH(S) from the mailing date of this action. 37 CFR 1.945. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.956.
For Third Party Requester's Comments on the Patent Owner Response:
30 DAYS from the date of service of any patent owner's response. 37 CFR 1.947. NO EXTENSIONS OF TIME ARE PERMITTED. 35 U.S.C. 314(b)(2).

All correspondence relating to this inter partes reexamination proceeding should be directed to the **Central Reexamination Unit** at the mail, FAX, or hand-carry addresses given at the end of this Office action.

This action is not an Action Closing Prosecution under 37 CFR 1.949, nor is it a Right of Appeal Notice under 37 CFR 1.953.

PART I. THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892
2. ☒ Information Disclosure Citation, PTO-1449 or PTO/SB/08
3. ☐ _____

PART II. SUMMARY OF ACTION:

1a. ☒ Claims 1-48 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled.
3. ☒ Claims 30 and 44 are confirmed. [Unamended patent claims]
4. ☐ Claims _____ are patentable. [Amended or new claims]
5. ☒ Claims 1-29, 31-43, and 45-48 are rejected.
6. ☐ Claims _____ are objected to.
7. ☐ The drawings filed on _____ ☐ are acceptable ☐ are not acceptable.
8. ☐ The drawing correction request filed on _____ is: ☐ approved. ☐ disapproved.
9. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119 (a)-(d). The certified copy has: ☐ been received. ☐ not been received. ☐ been filed in Application/Control No _____.
10. ☐ Other _____

1. The following is a response to patent owner's response under 37 § CFR 1.943 filed December 8, 2005. The third party requester has not filed a statement under 37 CFR § 1.947.

Information Disclosure Statements

2. MPEP § 609.05(a) states:

> If an item of information in an IDS fails to comply with all the requirements of 37 CFR 1.97 and 37 CFR 1.98, that item of information in the IDS will not be considered and a line should be drawn through the citation to show that it has not been considered.

3. Several documents listed on patent owner's multiple IDS submissions fail to comply with the requirements of 37 CFR § 1.98 and therefore have not been considered. The reasons for non-consideration are enumerated below.

IDS filed 11/28/2005

4. 37 CFR § 1.98(a)(2) states:

> (2) A legible copy of:
> (i) Each foreign patent;
> (ii) Each publication or that portion which caused it to be listed, other than U.S. patents and U.S. patent application publications unless required by the Office;
> (iii) For each cited pending unpublished U.S. application, the application specification including the claims, and any drawing of the application, or that portion of the application which caused it to be listed including any claims directed to that portion; and
> (iv) All other information or that portion which caused it to be listed.

The following list of documents are illegible as supplied and scanned into the office Image File Wrapper system. As such, patent owner did not submit a legible copy of the above documents as required by 37 CFR § 1.98(a)(2) and the listed documents have not been considered[1].

1 It is noted that document GJ as scanned into the present reexamination is also illegible. However, the file history of copending reexamination 95/000,089 was consulted and a more legible copy of document GJ was obtained from the copending file history. The obtained document copy is being forwarded to scanning to complete the file record of the current reexamination.

IDS Identifier	***Author or Title***
BZ	Undy et al.

A copy of each of the following listed documents could not be located among the thousands of pages of documents submitted by patent owner and scanned into the office Image File Wrapper system. As such, patent owner did not comply with the requirements of 37 CFR § 1.98(a)(2) because patent owner failed to supply a copy of the above documents. Therefore, these documents have not been considered[2].

IDS Identifier	***Author or Title***
AU	IEEE Draft Standard for "Scalable Coherent ..."
AV	IEEE Draft Standard for "High-Bandwidth Memory Interface ..."
AW	Gerry Kane et al.
GD	Data General AViiON ...

5. Note, in the following sections, parenthetical expressions of the form (¶ number) following section headings refer to the paragraph number of the previous action where the rejection that the section addresses can be located. Note that in most cases, only the first paragraph where the rejection may be found is cross referenced.

Rejections Maintained

Rejection of claims 1-4, 7-10, and 13-17 in view of Kohn et al. (¶ 17) - see pg. 19.

2 It is noted that document GK, "Expert Witness Report of Richard A. Killworth, Esq." could not be located within the documents suppled on this IDS. However, the file history of copending reexamination 95/000,089 was consulted, and a copy of document GK was obtained from the copending reexamination. The document copy is being forwarded to scanning to complete the file record of the current reexamination.

Rejection of claims 18-19, 27-29, 36, 43, and 48 in view of Ide/Toshiba (¶ 57) - see pg. 22.

Rejection of claim 36 in view of Ide/Toshiba (¶ 64) - see pg. 26.

Rejection of claims 46-47 in view of Ide/Toshiba and Fukaya/Hitachi (¶ 124) - see pg. 34.

Rejection of claim 39 in view of Ide/Toshiba and Feng (¶ 129) - see pg. 34.

2006Rejection of claims 31-34 in view of Ide/Toshiba and Watkins/Sun (¶ 133) - see pg. 36.

Rejection of claim 45 in view of Ide/Toshiba and the Tullsen/Multithreading article (¶ 136) - see pg. 38.

Rejection of claims 18-28, 36, and 43 in view of the Asprey/HP 7100 article and Ide/Toshiba (¶ 158) - see pg. 40.

Rejection of claim 46 in view of Asprey/HP7100 and the ILLIAC IV Programming Manual (¶ 164) - see pg. 41.

Rejection of claims 18-29 and 31-36 in view of the Knebel/HP7100LC article, the Lee/HP7100LC article, and Ide/Toshiba (¶ 170) - see pg. 42.

Rejection of claim 42 and 46 in view of the Knebel/HP7100LC article and the ILLIAC IV Programming Manual (¶ 173) - see pg. 44.

Rejection of claims 40-42 in view of Knebel/HP7100LC and the Watkins/Sun article (¶ 176) - see pg. 45.

Rejection of claim 45 in view of Knebel/HP7100LC, Ide/Toshiba, and Tullsen/Multithreading (¶ 178) - see pg. 45.

Rejection of claims 40-42 in view of Spaderna/Sharp and Watkins/Sun (¶ 208) - see pg. 46.

Rejection of claim 45 in view of Spaderna/Sharp and the Tullsen/Multithreading article (¶ 214) - see pg. 46.

Rejections withdrawn

Rejection of claims 30 and 44 in view of Ide/Toshiba (¶ 63) - see pg. 25.

Rejection of claims 18-19, 21-27, 29, 32-38, 43-44 and 48 in view of the Motorola 88110 User's Manual (¶ 69)- see pg. 27.

Rejection of claims 18-20, 22-26, 29, 31-38, 43-45, and 48 in view of the Papadopoulos/StarT article (¶ 77) - see pg. 28.

Rejection of claims 18, 27-36, and 46-47 in view of Spaderna/Sharp (¶ 79) - see pg. 29.

Rejection of claims 18-19, 21-26, 28-31, 33-36, 40, and 42-44 in view of the ILLIAC IV Programming Manual (¶ 81-82) - see pg. 29.

Rejection of claims 18, 27-29, 31-36, 43, and 45-46 in view of the S-1 Annual Report Vols. I and II (¶ 87-88) - see pg. 30.

Rejection of claims 18-29, 31-37, 39-44, 46, and 48 in view of the Tyler/AltiVec article and the AltiVec Manual (¶ 101) - see pg. 31.

Rejection of claims 46-47 in view of the Motorola 88110 User's Manual and the

Spaderna/Sharp article (¶ 144) - see pg. 38.

Rejection of claims 28, 30, and 46-47 in view of the Motorola 88110 User's Manual and the Fukaya/Hitachi patent (¶ 146) - see pg. 39.

Rejection of claims 39-42 in view of the Motorola 88110 User's Manual and Watkins/Sun article (¶ 151) - see pg. 39.

Rejection of claims 20 and 45 in view of the Motorola 88110 User's Manual and the Papadopoulos/StarT article (¶ 154) - see pg. 39.

Rejection of claim 45 in view of the Motorola 88110 User's Manual and the Tullsen/Multithreading article (¶ 156) - see pg. 40.

Rejection of claim 41 in view of ILLIAC IV and Watkins/Sun (¶ 189) - see pg. 45.

Rejection of claims 18, 27-29, 31-33, and 46 in view of Kimura/Fujitsu and Fujitsu '820 application (¶ 216) - see pg. 46.

Rejection of claim 45 in view of AltiVec and the Tullsen/Multithreading article (¶ 225) - see pg. 47.

Rejection of claims 30 and 47 in view of AltiVec and Fukaya/Hitachi (¶ 227) - see pg. 47.

Claims confirmed

6. Claims 30 and 44 are confirmed.

Revisions to prior office action

7. A review of the file history reveals that the decision in the order granting

reexamination to consider issues of statutory and obviousness double patenting as outside the scope of reexamination was in error. These issues should have been addressed in the prior action thereby giving patent owner and the third party requester rights to appeal the decisions. See MPEP § 2617. Accordingly, new rejections for statutory double patenting and an explanation regarding the obvious-type double patenting issue presented by the third party requester are set forth below.

8. As to the issue of obvious-type double patenting, the requester appears to be arguing that the change in priority date for parent '599 patent would not effect the validity term of the present patent due to the exclusion language of the terminal disclaimer (see second paragraph on pg. 1 of the terminal disclaimer filed on June 23, 2003 in the present patent). This language states that:

> "the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 to 156 and 173 of the prior patent, as presently shortened by any terminal disclaimer, in the event that it later:
>
> expires for failure to pay a maintenance fee,
>
> is held unenforceable,
>
> is found invalid by a court of competent jurisdiction,
>
> is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321,
>
> has all claims canceled by a reexamination certificate,
>
> is reissued,
>
> or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer."

The above exclusion language from the terminal disclaimer sets forth seven separate reasons why the term of the present patent will not be further disclaimed in the event that the parent patent ceases to be enforceable and/or has its term

shortened for any of the above seven enumerated reasons. In all cases, however, the language relates to excluding that part which would extend to the "full statutory term" of the prior patent should one or more of the events listed occur to the prior patent. In the present situation, the prior patent ('599') is a post GATT patent. Therefore, the "statutory term" of the prior patent is twenty years from the earliest claimed priority date. As the present patent claims priority as a continuation to the '599 patent, the "statutory term" of the present patent is identical to the "statutory term" of the prior '599 patent. When the prior patent's priority claim was modified certificate of correction, that changed the basis for calculating the "statutory term" of the prior patent. I.e., the prior patent received a new "statutory term" because the earliest claimed filing date of the prior patent changed. As the "statutory term" of the present patent is identical to the "statutory term" of the prior patent ('599), this modification in "statutory term" to the '599 patent also modified the "statutory term" of the present patent. So, if as the third party requester has indicated, the term of the parent patent ('599) changed from August 24, 2018 to August 16, 2015[3] because of the change to the priority claim to '599, then the "statutory term" of the present patent also changed to August 16, 2015.

Furthermore, the exclusion language of the terminal disclaimer indicates that patent owner did not disclaim the terminal part of the present patent that would extend to the full statutory term of the prior patent in the event that the prior patent ceased to be enforceable for one of the seven enumerated reasons.

3 These dates provided by the third party requester are unverified, and are simply being taken as accurate for the purpose of this explanation. The office is in no way making any statement as to the accuracy of these dates suppled by the third party requester.

However, the change which occurred to the statutory term of the prior patent is not one of the seven enumerated reasons. Therefore, the exclusionary language of the terminal disclaimer does not come into play because the change to the prior patent was not one of the exclusionary triggers. Accordingly, the change in term to the prior patent results in a corresponding equal change in term to the present patent.

New rejections

9. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. § 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. § 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. § 101.

10. Claims 2-6, 8-12, 14, and 17 are rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-12 of prior U.S. Patent No. 6,295,599. This is a double patenting rejection.

The claims overlap as shown in the tables below:

Patent: 6,725,356	***Patent: 6,295,599***
1. In a system having a data path functional unit having a functional unit data path width,	1. In a system having a data path functional unit having a functional unit data path width,
a first memory system having a first data path width,	a first memory system having a first data path width,
and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,	and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,
a method comprising:	a method comprising:
copying a first memory operand portion from the first memory system to the second memory system,	copying a first memory operand portion from the first memory system to the second memory system,
the first memory operand portion having the first data path width; and	the first memory operand portion having the first data path width;
copying a second memory operand portion from the first memory system to the second memory system,	copying a second memory operand portion from the first memory system to the second memory system,
the second memory operand portion having the first data path width and being catenated in the second memory system with the first memory operand portion,	the second memory operand portion having the first data path width and being catenated in the second memory system with the first memory operand portion,
thereby forming catenated data.	thereby forming catenated data; and
2. The method of claim 1 further comprising	
reading at least a portion of the catenated data which is greater in width than the first data path width.	reading at least a portion of the catenated data which is greater in width than the first data path width.
3. The method of claim 2 further comprising	2. The method of claim 1 further comprising
specifying a memory specifier from which a plurality of data path widths of data can be read.	specifying a memory specifier from which a plurality of data path widths of data can be read.

Patent: 6,725,356	***Patent: 6,295,599***
4. The method of claim 3 wherein the memory specifier comprises:	3. The method of claim 2 wherein the memory specifier comprises:
a memory address; a memory size; and a memory shape.	a memory address; a memory size; and a memory shape.
5. The method of claim 2 further comprising	4. The method of claim 1 further comprising
checking the validity of the first memory operand portion and, if valid, permitting a subsequent instruction to access the first memory operand portion.	checking the validity of the first memory operand portion and, if valid, permitting a subsequent instruction to access the first memory operand portion.
6. The method of claim 2 further comprising	5. The method of claim 1 further comprising
checking the validity of the second memory operand portion and, if valid, permitting a subsequent instruction to access the second memory operand portion.	checking the validity of the second memory operand portion and, if valid, permitting a subsequent instruction to access the second memory operand portion.

Patent: 6,725,356	***Patent: 6,295,599***
7. In a system having a data path functional unit having a functional unit data path width,	6. In a system having a data path functional unit having a functional unit data path width,
a first memory system having a first data path width,	a first memory system having a first data path width,
and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,	and a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,
a method comprising:	a method comprising:
copying a first memory operand portion from the first memory system to the second memory system,	copying a first memory operand portion from the first memory system to the second memory system,
the first memory operand portion having the first data path width;	the first memory operand portion having the first data path width;
copying a second memory operand portion from the first memory system to the second memory system,	copying a second memory operand portion from the first memory system to the second memory system,
the second memory operand portion having the first data path width; and	the second memory operand portion having the first data path width;
catenating the second memory operand portion in the second memory system with the first memory operand portion,	catenating the second memory operand portion in the second memory system with the first memory operand portion,
thereby forming catenated data.	thereby forming catenated data; and
8. The method of claim 7 further comprising	
reading at least a portion of the catenated data which is greater in width than the first data path width.	reading at least a portion of the catenated data which is greater in width than the first data path width.
9. The method of claim 8 further comprising	7. The method of claim 6 further comprising
specifying a memory specifier from which a plurality of data path widths of data can be read.	specifying a memory specifier from which a plurality of data path widths of data can be read.

Patent: 6,725,356	***Patent: 6,295,599***
10. The method of claim 9 wherein the memory specifier comprises:	8. The method of claim 7 wherein the memory specifier comprises:
a memory address; a memory size; and a memory shape.	a memory address; a memory size; and a memory shape.
11. The method of claim 8 further comprising	9. The method of claim 6 further comprising
checking the validity of the first memory operand portion and, if valid, permitting a subsequent instruction to access the first memory operand portion.	checking the validity of the first memory operand portion and, if valid, permitting a subsequent instruction to access the first memory operand portion.
12. The method of claim 8 further comprising	10. The method of claim 6 further comprising
checking the validity of the second memory operand portion and, if valid, permitting a subsequent instruction to access the second memory operand portion.	checking the validity of the second memory operand portion and, if valid, permitting a subsequent instruction to access the second memory operand portion.

Patent: 6,725,356	***Patent: 6,295,599***
13. In a system having a data path functional unit having a functional unit data path width,	11. In a system having a data path functional unit having a functional unit data path width,
a first memory system having a first data path width, and	a first memory system having a first data path width, and
a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,	a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,
a system comprising:	a system comprising:
a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system,	a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system,
the first memory operand portion having the first data path width; and	the first memory operand portion having the first data path width;
a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system,	a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system,
the second memory operand portion having the first data path width and	the second memory operand portion having the first data path width and
being catenated in the second memory system with the first memory operand portion,	being catenated in the second memory system with the first memory operand portion,
thereby forming catenated data.	thereby forming catenated data; and
14. The system of claim 13 further comprising	
a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.	a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.

Patent: 6,725,356	***Patent: 6,295,599***
15. In a system having a data path functional unit having a functional unit data path width,	12. In a system having a data path functional unit having a functional unit data path width,
a first memory system having a first data path width, and	a first memory system having a first data path width, and
a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,	a second memory system having a data path width which is greater than the functional unit data path width and greater than the first data path width,
a system comprising:	a system comprising:
a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system,	a first copying module configured to copy a first memory operand portion from the first memory system to the second memory system,
the first memory operand portion having the first data path width; and	the first memory operand portion having the first data path width;
a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system,	a second copying module configured to copy a second memory operand portion from the first memory system to the second memory system,
the second memory operand portion having the first data path width.	the second memory operand portion having the first data path width;
16. The system of claim 15 further comprising	
a catenating module configured to catenate in the second memory system the second memory operand portion with the first memory operand portion,	a catenating module configured to catenate in the second memory system the second memory operand portion with the first memory operand portion,
thereby forming catenated data.	thereby forming catenated data; and
17. The system of claim 16 further comprising	

Patent: 6,725,356	Patent: 6,295,599
a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.	a reading module configured to read at least a portion of the catenated data which is greater in width than the first data path width.

11. It should be noted that claims 1, 6, and 11-12 of prior patent '599 also anticipate claims 1, 7, 13, and 15 of the present patent. However, because anticipatory double patenting is an obviousness type double patenting, the existing disclaimer against the '599 patent is effective to render rejection of these claims under anticipatory double patenting moot.

12. Claims 18, 27-28, 31, 33-34, and 46-47 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 4, 9-11, 13, and 15 of US Patent 6,643,765. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1, 2, 4, 9-11, 13, and 15 of US Patent 6,643,765 anticipate claims 18, 27-28, 31, 33-34, and 46-47 of this patent.

> The non-statutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustifiied or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. *See In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
>
> A timely filed terminal disclaimer in compliance with 37 CFR § 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR § 1.130(b).
>
> Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1, 2, 4, 9-11, 13, and 15 of patent 6,643,765 contain every element of

claims 18, 27-28, 31, 33-34, and 46-47 of the instant application and as such anticipate claims 18, 27-28, 31, 33-34, and 46-47 of the instant application.

> "A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (Affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus)." *Eli Lilly and Company v. Barr Laboratores, Inc.* United States Court of Appeals for the Federal Circuit, on petition for rehearing en banc (Decided: May 30, 2001).

Patent: 6,725,356	***Patent: 6,643,765***
18. A method of processing a data stream in	1. A programmable media processor comprising:
a general purpose processor	a general purpose processor architecture,
capable of operation independent of another host processor,	capable of operation independent of another host processor,
the general purpose processor	
having a virtual memory addressing unit,	having a virtual memory addressing unit,
an instruction path and a data path	an instruction path and a data path;
to digitally process the data stream,	
the method comprising:	
	an external interface operable to
receiving the data stream	receive data
	from an external source and communicate the received data
over the data path;	over the data path;
	a cache operable to retain data communicated between the external interface and the data path;
storing partitioned data in registers of a register file coupled to the data path,	at least one register file configurable to receive and store data

Patent: 6,725,356	***Patent: 6,643,765***
	from the data path and to communicate the stored data to the data path; and
	a multi-precision execution unit coupled to the data path,
	the multi-precision execution unit configurable to
dynamically partitioning the data stream based on an elemental width of the data and	dynamically partition data received from the data path to account for an elemental width of the data
wherein a number of data elements stored in a register is inversely related to the elemental width of the data stored in partitioned fields of the register;	wherein the elemental width of the data is equal to or narrower than the data path,
	the multi-precision execution unit being capable of
performing group floating point operations on multiple operands stored in partitioned fields of registers and,	performing group floating-point operations on multiple operands in partitioned fields of operand registers and
for each group floating point operation,	
returning catenated results	returning catenated results.
of the operation to a register.	
28. The method of claim 18 wherein the performing step comprises	2. The media processor of claim 1 wherein the multi-precision execution unit is capable of
performing group add, group subtract and group multiply arithmetic operations on catenated floating-point data and, for each such group operation, returning catenated results of the operation to a register.	performing group add, group subtract and group multiply arithmetic operations on catenated floating-point data and, for each such group operation, returning catenated results of the operation to a register.

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27. The method of claim 18 wherein, for a specific group floating point operation performed, the catenated results of the specific operation are returned to a register that is different than the registers used to store the multiple operands for the specific operation.	4. The media processor of claim 3 wherein the result register is a different register than either the first or second operand registers.
46. The method of claim 18 wherein the performing step comprises performing group floating-point operations on data having a total aggregate width of 128 bits.	9. The media processor of claim 1 wherein the multi-precision execution unit is capable of performing group floating-point operations on catenated data having a total aggregate width of 128 bits.
47. The method of claim 18 wherein the performing step comprises performing group floating-point operations on data of more than one precision.	10. The media processor of claim 1 wherein the multi-precision execution unit is capable of performing group floating-point operations on floating-point data of more than one precision.
31. The method of claim 18 further comprising	11. The media processor of claim 1 wherein the multi-precision execution unit is capable of
performing group integer operations on multiple operands stored in partitioned fields of registers and,	performing group integer operations on multiple operands in partitioned fields of operand registers and
for each group integer operation,	
returning catenated results of the operation to a register.	returning catenated results to a register.
33. The method of claim 31 wherein the	13. The media processor of claim 12 wherein at least some

Patent: 6,725,356	***Patent: 6,643,765***
performing group integer operations comprises performing group add, group subtract and group multiply arithmetic operations on catenated integer data and,	of the group add, group subtract and group multiply arithmetic operations perform arithmetic operations on integer data stored in first and second operand registers and
for each such group operation,	
returning catenated results of the operation to a register.	return the catenated result to a result register.
34. The method of claim 31 wherein the	15. The media processor of claim 11 wherein, when
performing group integer operations comprises operating, in parallel, on multiple operands stored in partitioned fields of registers.	performing at least some of the group integer operations, the multi-precision execution unit operates on partitioned fields of operand registers in parallel and
	returns the catenated results to a register.

Response to patent owner's arguments

Rejection of claims 1-4, 7-10, and 13-17 in view of Kohn et al. (¶ 17) - Maintained

14. In the remarks at pg. 2, patent owner asserts:

A. That: "Claims 1-17 require catenation of 2 operands of data path width, to form a wide operand -- that is, an operand wider than the functional data path. ... Kohn does not disclose or suggest forming a wide operand by catenating data as required by claims 1-4, 7-10 and 13, 14, 16 and 17 [sic]. In fact, the Kohn article (and the Intel i860 processor in general) contains no suggestion about handling wide operands. ... The rejection correlates the second memory system of the claims *(i.e.*, wider than the functional unit data path) with the 128-bit wide data path to the memory cache of Kohn. ... There is nothing in Kohn, however, that suggests that these multiple operand values can be catenated into a single larger wide operand for processing by the functional execution units with a single instruction."

This argument is not persuasive because patent owner's argument that Kohn et al. does not catenate multiple operand values into a single larger wide operand for processing by the execution units is also applicable to patent owner's broad claim language. The only mention within claim 1 of a functional unit is that there is a data path functional unit having a particular data path width. Beyond the mere mention of the presence of a functional unit within the claim preamble, there is no mention and no usage by the method of the functional unit. The claim copies two pieces of data from a first memory to a second memory where the first memory is of the same width as the function unit width and the second memory is wider than the function unit width. During this copying, the two pieces of data are catenated (placed together) in the second memory, to form only "catenated data". The claim does not state, and therefore, does not require, that this "catenated data" form any operand for any functional unit. Patent owner is reading limitations into the claims and therefore arguing limitations that are not present within the claim language, which is improper:

> Claimed subject matter, <u>not</u> the specification, is the measure of invention. Limitations in the specification <u>cannot</u> be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be **confused with adding an extraneous limitation** appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989) (citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

Patent owner appears to be placing some significance upon this argued "wide operand" term, however there is no such language or term anywhere within claim 1. Nor is the term "wide operand" utilized in any of claims 2-17. Accordingly, this argued significance of "wide operand" can not serve to overcome the rejection of claims 1-17 in view of Kohn et al. and the rejection is maintained.

Finding of lack of continuity to parent application (¶ 35) - Withdrawn

15. Patent owner's remarks covering pgs. 4-12 in favor of the claim for priority benefit of the parent application under 35 USC § 120 are convincing. The claims in this patent claim a method of operation, and patent owner's specification and appendix supplied with the parent application show both enablement for the method and adequate written description of the method to show that patent owner had possession of the method at the time of filing the parent application. Accordingly, this finding is withdrawn.

Rejection of claims 18-19, 27-29, 36, 43, and 48 in view of Ide/Toshiba (¶ 57) - Maintained

16. In the remarks at pg. 13-15, patent owner asserts:

A. That: "Ide does not disclose dynamic partitioning ...

Claim 18 requires more than just partitioning data; it requires partitioning of data that is ***dynamic*** to account for an elemental width of the data. ...

By contrast, Ide et al. discloses a non-dynamic way of partitioning data based on the rigid use of two execution modes -- the "scientific mode" and the "real-time mode." When placed in the scientific mode, the floating point processing unit (FPU) of Ide et al. treats 64-bit data as a single 64-bit operand. When placed in the real-time mode, the processing unit treats 64-bit data as two 32-bit operands. Once placed in a particular mode, the processing unit always partitions data in the manner conforming to that mode. *See* Ide et al., p. 352, col. 2, line 33 through p. 353, col. 1, line 7; and p. 356, col. 2, line 12 through p. 357, col. 1, line 8. ...

Once placed in a particular mode, the FPU partitions data in a fixed (*i.e.*, non-dynamic) way, no matter what instruction is issued. ... The partitioning of data can be changed only by switching the FPU into a different execution mode."

This argument is not persuasive because patent owner is importing limitations into the claim language which do not exist within the claims:

Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be **confused with adding an extraneous limitation** appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989) (citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from

> any need to interpret ... particular words or phrases in the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

Patent owner's comments amount to an assertion that a patent owner's perceived manner of operation of Ide et al. to provide dynamic partitioning does not read upon the claimed statement "dynamically partitioning". However, as seen from patent owner's claim 18, the claims merely state: "dynamically partitioning the data stream ...". The claim language makes no restriction to what particular manner of partitioning is considered to cover this claimed dynamic partitioning. As such, the broadest reasonable interpretation of the claim language is that it covers all manners of performing dynamic partitioning. As the ordinary and customary meaning of dynamic in the computer processor arts is occurring at the time of execution, patent owner's claims cover any form of partitioning that occurs at the time of execution. Patent owner presents an entire scenario detailing one example of how Ide et al.'s partitioning may operate on pg. 14 of the reply. As the entire scenario presented by patent owner occurs at the time of execution it is by definition dynamic, and accordingly, is a dynamic partitioning. Furthermore, Ide et al. at pg. 356, in the first sentence that begins the first paragraph of section V states:

> "The ALU and the MDU can execute operations in each cycle not only upon a set of data, but also upon two sets of single-precision data concurrently, by using the original twin single format"

Because Ide et al. states that the system can execute either upon one set, or upon two sets, of data "in each cycle", Ide et al. is specifically referring to an at execution time system, and as such, is "dynamic" as that word is ordinarily and customarily used in the computer processor arts.

17. In the remarks at pgs. 15-16, patent owner asserts:

> That: "Ide does not disclose a virtual memory addressing unit
>
> Ide also fails to disclose a virtual memory addressing unit as recited in claim 18. The Rejection points to the mention of a 'memory management unit' in Ide et al. as purportedly disclosing this feature. ... However, such a 'memory management unit' (MMU) is simply a unit that controls the assignment and usage of memory by the processor. ... Ide only mentions "memory management unit" once in passing. ... No further detail is provided. ... Thus, it cannot be presumed that the 'memory management unit' mentioned in Ide provides any virtual memory capability.

Patent owner's argument is not persuasive because the industry accepted meaning of "memory management unit" as found from the en.wikipedia.org definition for "memory management unit" clearly indicates that a memory management unit is accepted as implementing virtual memory as known to those of skill in the art:

> "**MMU**, short for **Memory Management Unit**, is a class of computer hardware components responsible for handling memory accesses requested by the CPU. Among the functions of such devices are the translation of virtual addresses to physical address (i.e., **virtual memory management**) ..." <http://en.wikipedia.org/wiki/Memory_Management_Unit> (emphasis added)

Furthermore, the definition for "memory management unit" found from the foldoc.org web site contains the following as its first sentence:

> "**Memory Management Unit** <hardware, memory management> (MMU, "Paged Memory Management Unit", PMMU) A hardware device or circuit that supports virtual memory ..." dated 1999-05-24 <http://foldoc.org/?query=memory+management+unit&action=Search>

Accordingly, the art recognized ordinary and customary meaning for "memory management unit" is a device that implements virtual memory. Therefore, Ide et al.'s teaching of a "memory management unit" taught virtual memory.

18. In the remarks at pg. 16, patent owner asserts:

> That: "Ide does not disclose a general purpose processor

> Ide also fails to disclose a general purpose processor architecture capable of operation independent of another host processor and which includes the recited claim limitations, such as a virtual memory addressing unit. Instead Ide discloses an FPU that was designed to be tightly coupled to a RISC core. ... Beyond merely stating this objective, Ide discloses little regarding the operational capabilities or architecture of such a RISC core.

Initially, patent owner's argument regarding a lack of a virtual memory addressing unit is simply a repeat of the argument of pgs. 15-17 of the response, and have been fully dealt with above beginning at pg. 24 above. As to patent owner's argument regarding a single general purpose processor architecture, patent owner has simply failed to understand what Ide et al. is teaching from the cited paragraphs. The first paragraph of col. 1 of pg. 352 of Ide et al. is teaching that existing RISC processors, which are "single general purpose processors" contain, inter alia, floating point units integrated on board the RISC processor. The third paragraph of col. 1 of pg. 352 of Ide et al. is indicating that the FPU disclosed in the remainder of Ide et al. is suitable for use as the FPU that is integrated on board one of those existing RISC processors. Accordingly, Ide et al. is teaching that the disclosed FPU should be integrated on board an existing RISC processor, and as a result, disclosed a "single general purpose processor" which contained the claimed elements.

Rejection of claims 30 and 44 in view of Ide/Toshiba (¶ 63) - Withdrawn

19. In the remarks at pgs. 16-17, patent owner asserts:

> That: "Dependent claim 30 requires performing group floating-point operations on data of two different precision. The Office Action relies upon Fig. 9(a) if Ide for this feature. ... However, the 64-bit operation of Ide is not a group operation pursuant to claim 30 because Ide only operates on a single operand in 64-bit mode (only K+L).

> Thus, Ide does not teach performing group floating-point operations on data of two different precisions, as per claim 30."

Patent owner's argument is persuasive in that when "group" is taken with its ordinary and customary meaning of two or more items that Ide et al.'s 64-bit operation mode is not a group operation because it does not operate upon two or more more elements. Accordingly, the rejection of claim 30 in view of Ide et al. is withdrawn. As claim 44 recites identical claim text to claim 30, the rejection of claim 44 is also withdrawn for the same reasons.

Rejection of claim 36 in view of Ide/Toshiba (¶ 64) - Maintained

20. In the remarks at pg. 17, patent owner asserts:

> That: "Dependent claim 36 requires group data handling operations, and claim 44 further require group data handling operations for data of two different precisions. The Office Action cites Figs. 9(a) and 9(b) of Ide for these features. ... Ide Fig. 9(a) does not describe group data handling operations, but instead refers to arithmetic operations. ... Thus, those figures do not teach the claimed 'group data handling operations.' ... Further, it is clear that Ide does not disclose group data handling operations on data of different precisions, and thus claim 44 is patentable for this additional reason."

This is not found persuasive because patent owner is attaching a meaning to "group data handling operations" that is not required to understand the meaning of the term in the claim language. The claim language places no restriction on what kinds of operations constitute a claimed "operation" nor upon what kinds of "data handling" constitute a claimed "data handling". Furthermore, patent owner appears to be placing some significance upon the term "handling" by implying that an arithmetic operation is not a data handling operation. However, the claimed term "data handling" is significantly broader than "arithmetic" and as such, encompasses

within its scope not only arithmetic operations, but other operations that are not arithmetic operations. As Ide et al. Figs. 9(a) and 9(b) show "operations" (arithmetic) by "handling" (arithmetic) "data" (input operands) as a "group" (two data values in parallel), the figures show "group data handling operations. Therefore, for at least the very broad recitation of claim 36, Ide et al. discloses at least one aspect that fits within the boundaries set out by the broad claim language recitation of "data handling".

As to claim 44, the rejection of that claim was withdrawn above and no further comment herein is deemed necessary.

Rejection of claims 18-19, 21-27, 29, 32-38, 43-44 and 48 in view of the Motorola 88110 User's Manual (¶ 69) - Withdrawn

21. In the remarks at pg. 17-21, patent owner asserts:

> That: "Motorola's PCMP instruction does not return catenated results from a group floating-point operation.
>
> Claim 18 requires performing group floating-point operations on multiple operands in partitioned fields and returning catenated results. ... Motorola's PCMP instruction does not return 'catenated results'. That is, the PCMP instruction does not return a set of answers generated by applying the *same* operation individually and separately to *each* operand in a partitioned field (or each pair of operands, for two-input operations). Instead, each individual answer returned by the PCMP instruction is actually generated by applying a *different* operation performed on *all* of the operands in the various fields of the operand registers."

Patent owner's argument against the Motorola reference contains one flaw. Patent owner summarizes the argument as Motorola does not return catenated results when in fact Motorola does return catenated results (several results packed together into a single output word). The difference between patent owner's claimed

invention and Motorola's PCMP instruction lies not in the "catenated results" but in the fact that Motorola arrives at the "catenated results" in a manner different from that with which patent owner arrives at their "catenated results". Furthermore Motorola performs different operations upon each each operand to arrive at the catenated results while the definition for "group operations" (¶ 11) in patent owner's claims is that the **same operation** is to be applied to each operand to arrive at the catenated results. Accordingly, although patent owner summarized the difference incorrectly, patent owner did identify a difference between their claim language and the Motorola reference. Accordingly, the rejection in view of Motorola is withdrawn.

Rejection of claims 18-20, 22-26, 29, 31-38, 43-45, and 48 in view of the Papadopoulos/StarT article (¶ 77) - Withdrawn

22. In the remarks at pg. 21-22, patent owner asserts:

> That: "Papadopoulos (Start Article) Fails to Anticipate Claims 18-20, 22-26, 29, 31-38, 43-45 and 48 ... The Office Action states that 'Requester's proposed rejection of claims 18-20, 22-26, 29, 31-38, 43-45 and 48 [with respect to the Papadopoulos/StarT Article] are adopted as presented on pages 40-41 of the Request.' Office Action, paragraph 77 (emphasis added). Pages 40-41 of Intel's Request for *Inter Partes* Reexamination states:
>
> > **'the Papadopoulous/StarT Article describes a [Motorola] 88110 [processor] with added features (referred to as '88110XP'). Since [the] Motorola 88110 is described and illustrated in the Papadopoulos/StarT Article, all of the inherent characteristics of the 88110 are also present. Therefore, for the same reasons as discussed above in paragraph 14 [with respect to the Motorola 88110 User's Manual], the Papadopoulos/StarT Article anticipates claims 18-20, 22-26, 29, 31-38, 43-45 and 48." Request, paragraph 15, pages 40-41 (emphasis added).** ... As described above, Motorola does not teach the step of "performing group floating point operations on multiple operands stored in partitioned fields of registers" as required by claim 18 and also does not teach the step of returning catenated results. Thus, because the entirety of the rejection of claims 18-20, 22-26, 29, 31-38, 43-45 and 48 is based on features associated with the Motorola 88110 processor, the Patent Owner

> respectfully asserts that the Papadopoulos/StarT article fails to anticipate these claims for all of the same reasons set forth in Section V above." (emphasis unchanged)

Patent owner's arguments regarding the Papadopoulos/StarT article are convincing, and for the same reasons above that Motorola did not anticipate the claims, the Papadopoulos/StarT article also fails to anticipate the claims.

Rejection of claims 18, 27-36, and 46-47 in view of Spaderna/Sharp (¶ 79) - Withdrawn

23. In the remarks at pg. 22-24, patent owner asserts:

> That: "Sharp fails to anticipate claims 18, 27-36 and 46-47 ... Sharp does not disclose a virtual memory addressing unit ... The Sharp floating point vector processor does not include a virtual memory addressing unit ... In this reexamination, the Requester has failed to show the Sharp processor includes a virtual memory addressing unit. The Requester only refers to pages 8 and 9 of Sharp, *see* Request at pg. 41-42 and claim chart CC-G, but nowhere is there any mention of a virtual memory addressing unit. ... The reason for this omission is clear -- Sharp simply does not have a virtual memory addressing unit."

Patent owner's argument regarding the Sharp reference is convincing in that the requester has failed to show where in Sharp can be found a virtual memory addressing unit. Therefore, the rejection of claims 18, 27-36, and 46-47 in view of Sharp is withdrawn.

Rejection of claims 18-19, 21-26, 28-31, 33-36, 40, and 42-44 in view of the ILLIAC IV Programming Manual (¶ 81-82) - Withdrawn

24. In the remarks at pg. 30-32, patent owner asserts:

> That: "ILLIAC fails to anticipate claims 18, 19, 21-26, 28-31, 33-36, 40, and 42-44 ... ILLIAC fails to disclose a general purpose processor capable of operation independent of another host processor ... ILLIAC also fails to disclose the processing

> of a data stream in a general purpose processor capable of operation independent of another host processor, as recited in claim 18. ... The rejection focuses on the PU's (in particular, the processing elements (PEs)) as processing the data stream. However, the PUs are not capable of operation independent of another host processor. In fact, the PUs are inoperable unless they are connected and controlled by the CUs. *See, e.g.*, ILLIAC, p. 1-11, paragraph 1 ('Each Control Unit (CU) directly controls a subarray of 64 Processing Units (PU) in a quadrant.'), p. 1-7, paragraph 1 ('The Control Unit is that portion of the computer system which performs the initial processing of instructions up to and including the generation of instruction microsequences for a step-by-step control of the Processing Element"), and p. 1-7 to 1-19 generally. The CUs, in turn, can only operate under the control of the B6700 control computer. *See id.*, p. 1-5 ('Is is this link that the B6700 uses to initialize the state word in each CU, that is setting the initial value of the program counter, the control state, and array configuration ... The B6700 also generates controls to initiate the transfer of programs and operands from disk to array memory before allowing the CUs to proceed with program execution'). Thus, the PUs that form the basis of the rejection depend on both the CUs and the P6700 [sic] control computer for operation."

Patent owner's arguments regarding the ILLIAC reference are persuasive and the rejection of claims 18, 19, 21-26, 28-31, 33-36, 40, and 42-44 in view of the ILLIAC reference are withdrawn. The ILLIAC processing elements (PEs) are not capable of operation independent of another host processor. Therefore this rejection is withdrawn.

Rejection of claims 18, 27-29, 31-36, 43, and 45-46 in view of the S-1 Annual Report Vols. I and II (¶ 87-88) - Withdrawn

25. In the remarks at pgs. 34-42, patent owner asserts plural reasons why they believe that the S-1 Annual Report (Exhibits PA-I,1 and PA-I,2) do not in fact anticipate the claims. For at least the reasons presented that the complex arithmetic operations are not performed on operand stored in partitioned fields of registers, and that vector operands are required to be stored in memory, not registers, the S-1 Annual Reports fail to disclose at least the claimed features of

storing partitioned data in registers and performing group floating point operations on multiple operands stored in partitioned fields of registers.

Rejection of claims 18-29, 31-37, 39-44, 46, and 48 in view of the Tyler/AltiVec article and the AltiVec Manual (¶ 101) - Withdrawn

26. Patent owner's arguments in favor of their priority claim has resulted in a withdrawal of the finding of lack of continuity to the parent application presented in the previous office action. As a result, rejections based upon intervening references, such as Tyler/AltiVec and the AltiVec Manual are withdrawn as not having a publication date sufficient to qualify as valid prior art against the claims.

Rejection of claims 21-26, 31-35, and 37-38 in view of Ide et al. and Diefendorff et al. (¶ 108) - Maintained

27. In the remarks at pg. 43, patent owner asserts:

> That: "Paragraph 109 of the Office Action states that 'Claims 21-26, 31-35, and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ide et al. in view of Diefendorff et al.' Diefendorff is a Motorola patent. For at least three reasons, this obviousness rejection should be withdrawn. First, in the '765 reexamination proceeding, the examiner rules that the Motorola teachings and the Ide reference were not combinable under § 103. (See '765 Office Action, dated 06/01/06, at paragraphs 77-78 and 93-98; ... This ruling and its rationale should apply to the '365 Reexamination as well."

Patent owner appears to have misinterpreted and, as a result, misunderstood the meaning of the cited paragraphs from the '765 reexamination. The ruling in the '765 reexamination was that the reasoning presented by the third party requester did not show a prima facie case for combination. The ruling in no way was a ruling

as to whether the references **could** be combined in some other manner and for some other reason.

28. In the remarks at pg. 43, patent owner asserts:

> That: ""Second, as to the motivation to combine, there is no disclosure in Ide that would suggest the alleged combination, especially because the Motorola disclosures teach away from combining the Motorola processor with a separate FPU. The Motorola disclosures teach away from the combination because they already had a capable floating-point unit. Given these pre-existing floating-point capabilities, most of the features provided by the FPU disclosed in Ide would be redundant to the capabilities already provided by the Motorola references, making it unlikely that anyone knowing of the floating-point capabilities already provided by the Motorola references would be motivated to add the capabilities of the Ide FPU."

This argument on the part of patent owner is not persuasive because the requirements for an obviousness rejection do not include a requirement that either particular reference explicitly suggest the combination. The test of obviousness is:

> "whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," In re Gorman, 933 F.2d at 986, 18 USPQ2d at 1888.
>
> Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).
>
> "Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." In re Wood, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).
>
> "In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found in a specific reference."
>
> Entire quote from In re Oetiker, 24 USPQ2d 1443 (CAFC 1992).
>
> "A suggestion, teaching, or motivation to combine the relevant prior art teachings does not have to be found explicitly in the prior art, as the teaching, motivation, or suggestion may be implicit from the prior art as a whole, rather than expressly stated in the references. . . . The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000)" *In re Leonard R. Kahn* (CAFC, 04-1616, 3/22/2006)

Furthermore, as to patent owner's assertion of teaching away, patent owner has provided no clear reasoning as to how one of ordinary skill would be discouraged from the path set out by the references.

> "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)." *In re Leonard R. Kahn* (CAFC, 04-1616, 3/22/2006)

Patent owner has presented nothing more than the statement that because both Ide et al. and Motorola each have floating point units, that Motorola teaches away from the combination. The mere fact that Motorola already had a floating point unit does not teach away from a combination when Ide et al. taught a more powerful floating point unit as detailed by the third party requester (68 MFLOPS for Motorola's original FPU vs. 320 MFLOPS for Ide et al.'s enhanced FPU). Certainly the increased computational power (4.7 times more performance) afforded by the Ide et al. FPU design is a clear motivating factor for combination to one of ordinary skill in the art.

29. In the remarks at pg. 43, patent owner asserts:

> That: "Third, the alleged combination does not teach may of the claim limitations. For example, claim 33 requires, in part, performance of 'group multiply arithmetic operations.' The Motorola pmul instruction identified in Requesters claim chart fails to disclose this limitation. Instead, the pmul instruction i simply a plain multiply operation that multiplies two numbers together to generate a single result. *See* Motorola at 10-65 for definition of pmul instruction."

Patent owner's argument in support of claim 33 is not convincing because claim 33 requires group integer operations, something detailed by Motorola at fig. 5 on pg. 64 where the pmul instruction is diagrammed as multiplying a value against four packed pixel components. A clearer picture of the same figure can be found at

pg. 5-25 of the Motorola MC88110 user's guide document.

As to the other claims, patent owner has not identified any particular specific claim limitations which are not found by the combination of references. Accordingly, having identified no missing claim language elements, it can only be presumed that all of the remaining claim elements are taught by the references.

Rejection of claims 46-47 in view of Ide/Toshiba and Fukaya/Hitachi (¶ 124) - Maintained

30. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claim 39 in view of Ide/Toshiba and Feng (¶ 129) - Maintained

31. In the remarks at pg. 43-44, patent owner asserts:

> That: "No motivation exists to combine Toshiba and Feng ...
>
> Contrary to the Requesters reasoning, Patent Owner submits that Toshiba and Feng are directed to different problems. Toshiba describes a floating-point unit (FPU) for superscalar processors. The FPU is designed to be tightly coupled with a RISC core and adopts a RISC approach to meet speed requirements. Two execution modes are disclosed to meet precise scientific computations and real-time applications. Toshiba discloses a new exception prediction technique to make effective use of machine parallelism. All the operations that were envisioned for the FPU are described by Toshiba, and accordingly, there is no motivation for one of ordinary skill in the art to incorporate the data manipulation circuits disclosed by Feng into the Toshiba FPU."

Patent owner's argument against the combination of Toshiba and Feng can be summarized as: because Toshiba created a functioning FPU, there is no motivation

to further modify the FPU. If this were the standard for obviousness, then nothing would ever be obvious, and if this were the standard that were applied by those of skill in the art working in industry, there would never be any new inventions created. Patent owner's argument can also be summarized as: because Toshiba envisioned operations X, Y, and Z for their FPU, there would be no reason to further modify the FPU. This argument is also flawed for the exact same reason presented above on pg. 33.

In the case of the Feng publication, the publication is directed to various functions for manipulating data in parallel processors in general. That means that the Feng publication suggests to one of ordinary skill in the art that his teachings are applicable to any parallel processor. As Toshiba provides a parallel processing capability in their FPU, one of ordinary skill in the art would have recognized a nexus between Feng's teachings and Toshiba's FPU due to the parallel processing nature. Furthermore, Feng continues by disclosing that in order to further increase processing speed in processors, more than simply increasing the clock speed must be performed (pg. 89-90, Introduction section), and suggests that performing parallel processing on plural words simultaneously is one solution to obtaining greater performance. Because Toshiba disclosed a parallel processing architecture for performing parallel processing on plural words simultaneously in their FPU, one of skill in the art would be immediately motivated to apply Feng's teachings to Toshiba's FPU in order to further enhance the Toshiba FPU's performance, as

suggested by Feng.

32. In the remarks at pg. 44-45, patent owner asserts:

> That: "Even if combined, the combination fails to disclose the limitations of claim 39
> Claim 39 requires that data elements from two separate operand registers be interleaved. Patent owner submits that such interleaving, as recited in claim 39, is not disclosed by Feng."

Patent owner's attention is directed to pg. 97 of Feng, in the section labeled "Appendix A, DMF Glossary". In this section Feng details the meaning of "MERGE" as "interleaving two or more ordered subgroups of elements into one ordered group". This is exactly the same operation as that claimed by claim 39. Accordingly, Feng does indeed teach the limitations of claim 39.

Rejection of claims 31-34 in view of Ide/Toshiba and Watkins/Sun (¶ 133) - Maintained

33. In the remarks at pg. 45, patent owner asserts:

> That: "The rejection of claims 31-34 for obviousness (35 U.S.C. § 103) based on the teachings of Ide and Watkins is respectfully traversed. ... The sole basis for referring to Watkins for claims 31-34 is for its alleged group integer operations on graphics data. ... The SX pixel processor referenced in the Watkins et al. article "acts as a coprocessor to a CPU." Watkins at 326, right-hand column. Taking Watkins and Ide in combination yields a floating point unit (Ide) and a graphics coprocessor (Watkins). How these two co-processing units meet the requirement of a general purpose processor in base claim 18 (and thus claims 31-34) remains unanswered."

Patent owner's argument against the combination of Ide et al. and Watkins et al. is arguing that it is not obvious to combine the two references because they can not be bodily incorporated into one another. However, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be

expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, Watkins taught that having vector shift instructions was advantageous in a media processing environment (see Watkins, pg. 324, col. 2, first full paragraph: "The SX Pixel Processor (SXPP) has an instruction set which is tailored to the needs of image processing and multi-media applications as well as 2D and 3D graphics", emphasis added) such as that envisioned by Ide et al.

34. In the remarks at pg. 45-46, patent owner asserts:

> That: "Claim 31 requires 'group integer operations on multiple operands stored in partitioned fields of registers and ... returning catenated results.' Watkins' vector shift instructions only shift vector elements contained in *separate registers*, not data elements catenated in *an* operand register."

Patent owner continues this argument with an explanation relating to the manner within which Watkins et al. processes vectors through a paired ALU arrangement and argues that because of this arrangement, claim 31 is not disclosed by Watkins et al. Patent owner is reminded that claim 31 is a method claim, this means that claim 31 is claiming the steps or function performed by the hardware, and not the actual hardware itself. In the case of claim 31, the claim broadly recites that the function to be performed is that of performing group integer operations and returning catenated results. This broad claim language makes no mention of how this particular function is performed, nor does this broad claim language make any mention of any particular hardware structure layout to perform this function.

Therefore, any hardware structure that performs the same function reads upon the broad language of claim 31. In the case of Watkins et al., the reference discloses performing the functions of group integer operations at the previously cited locations within the reference. As to the argument that Watkins et al. places each element in a separate register, patent owner's attention is directed to table 3 on pg. 335 which shows that for the "8-bit (packed)" memory pixel format, Watkins et al. does indeed store plural elements concatenated in a single register ("4 8-bit pixels to one register").

Rejection of claim 45 in view of Ide/Toshiba and the Tullsen/Multithreading article (¶ 136) - Maintained

35. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claims 46-47 in view of the Motorola 88110 User's Manual and the Spaderna/Sharp article (¶ 144) - Withdrawn

36. Patent owner's arguments as to why the Motorola 88110 User's manual does not disclose features of claim 18 result in the Motorola 88110 User's manual also not disclosing features necessary for the rejection of claims 39-42 which all depend from claim 18. Therefore the rejection of claims 39-42 in view of the Motorola 88110

User's Manual and Watkins/Sun are withdrawn.

Rejection of claims 28, 30, and 46-47 in view of the Motorola 88110 User's Manual and the Fukaya/Hitachi patent (¶ 146) - Withdrawn

37. Patent owner's arguments as to why the Motorola 88110 User's manual does not disclose features of claim 18 result in the Motorola 88110 User's manual also not disclosing features necessary for the rejection of claims 28, 30, and 46-47 which all depend from claim 18. Therefore the rejection of claims 28, 30, and 46-47 in view of the Motorola 88110 User's Manual and the Fukaya/Hitachi patent are withdrawn.

Rejection of claims 39-42 in view of the Motorola 88110 User's Manual and Watkins/Sun article (¶ 151) - Withdrawn

38. Patent owner's arguments as to why the Motorola 88110 User's manual does not disclose features of claim 18 result in the Motorola 88110 User's manual also not disclosing features necessary for the rejection of claims 39-42 which all depend from claim 18. Therefore the rejection of claims 39-42 in view of the Motorola 88110 User's Manual and Watkins/Sun are withdrawn.

Rejection of claims 20 and 45 in view of the Motorola 88110 User's Manual and the Papadopoulos/StarT article (¶ 154) - Withdrawn

39. Patent owner's arguments as to why the Motorola 88110 User's manual does not disclose features of claim 18 result in the Motorola 88110 User's manual also not

disclosing features necessary for the rejection of claims 20 and 45 which all depend from claim 18. Therefore the rejection of claims 20 and 45 in view of the Motorola 88110 User's Manual and the Papadopoulos/StarT patent are withdrawn.

Rejection of claim 45 in view of the Motorola 88110 User's Manual and the Tullsen/Multithreading article (¶ 156) - Withdrawn

40. Patent owner's arguments as to why the Motorola 88110 User's manual does not disclose features of claim 18 result in the Motorola 88110 User's manual also not disclosing features necessary for the rejection of claims 45 which all depend from claim 18. Therefore the rejection of claims 45 in view of the Motorola 88110 User's Manual and the Tullsen/Multithreading article are withdrawn.

Rejection of claims 18-28, 36, and 43 in view of the Asprey/HP 7100 article and Ide/Toshiba (¶ 158) - Maintained

41. In the remarks at pg. 49, patent owner asserts:

> That: "There is no motivation to combine Asprey and Ide because Asprey specifically shunned the use of highly parallel algorithms in the PA7100 floating point unit because of concerns regarding circuit density, and this functionality 'could not be compressed onto the CPU die.' Asprey at 28. ... One of the basic, functional design goals of Asprey (HP) was to develop the PA7100 for low-cost applications. The Toshiba FPU was a very customized circuit that required extensive layout design and simulation. One skilled in the art would not have been motivated to dissect the HP PA7100 processor, extract the simple, inexpensive, floating point unit of that processor, and replace it with the highly complex Toshiba design."

Patent owner's argument above appears to be in part that Asprey teaches away from replacing the floating point unit with a different design. However, patent owner's argument has not met the requisite requirements for teaching away from

the combination:

> "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)." *In re Leonard R. Kahn* (CAFC, 04-1616, 3/22/2006)

The relevant portion of Asprey et al. cited by patent owner does not discourage one of ordinary skill in the art from making the proposed modification to Asprey et al. Quite the contrary, it simply states why Asprey et al. made the choices they made. If the cited portion does anything, it is a clear suggestion to one of skill in the art to make modifications once integrated circuit technology advanced to the point that the modifications would fit within the chip level transistor budget for that chip technology.

42. In the remarks at pg. 49, patent owner asserts:

> That: "Additionally, even if combinable, the references do not teach the claim limitations. As discussed in detail above, Ide fails to disclose the step of 'dynamically partitioning data,' as recited in claim 18."

This argument is not persuasive. It has been addressed in detail above starting on page 22.

Rejection of claim 46 in view of Asprey/HP7100 and the ILLIAC IV Programming Manual (¶ 164) - Maintained

43. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claims 18-29 and 31-36 in view of the Knebel/HP7100LC article, the Lee/HP7100LC article, and Ide/Toshiba (¶ 170) - Maintained

44. In the remarks at pgs. 50-52, patent owner asserts:

> That: "No motivation exists to combine Toshiba, Knebel, and Lee
>
> One of ordinary skill in the art would not have been motivated to incorporate the floating point unit (FPU) of Toshiba in PA7100LC since doing so would invariable increase the complexity of the PA7100LC thereby leading to increased costs, increased chip size ... and increased power consumption -- the very thing HP was seeking to avoid in the 7100LC. The clearly stated design goals of the PA7100LC processor was to provide a low cost processor with reduced chip size and power consumption characteristics, as repeatedly mentioned in Knebel and Lee. Incorporating the Toshiba FPU into the PA7100LC would in fact vitiate the intended purpose of the PA7100LC. Accordingly, not only is there no motivation to incorporate the FPU of Toshiba into the PA7100LC disclosed by Knebel and Lee, the Knebel and Lee references in fact teach away from such a combination."

This argument is not persuasive for two reasons. First, as to the sub-argument regarding teaching away, the cited portions of the references do nothing of the sort:

> "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994)." *In re Leonard R. Kahn* (CAFC, 04-1616, 3/22/2006)

Nothing within the cited portions of Knebel and Lee specifically discourage one of skill in the art from making the proposed modification. The cited sections in fact teach in favor of making the modification because they indicate aspects that Knebel and Lee would have preferred to implement but could not given the technology constraints at the time of their invention.

Secondly, obviousness for patent owner's claims is not measured at the time of HP's invention, but at the time of patent owner's invention, which is a date at least several years later than the date of HP's invention. Because of advancements

in semiconductor technology in the intervening years, one of skill in the art would be motivated to create a modified version of the PA7100LC that contained enhanced features such as that taught by Toshiba while maintaining all the low power and low costs associated with Knebel and Lee's disclosures.

45. In the remarks at pg. 52, patent owner asserts:

> That: "Further, Knebel states that '[g]iven the excellent floating-point performance of the PA7100, the design focus for the PA7100LC floating-point was to leverage as much as possible from the PA7100 while reducing power consumption and chip area.' *See* Knebel at 442. The excellent floating point capabilities of the PA7100 thus met and satisfied all the floating point processing requirements envisioned by the designers for the PA7100LC. Given the excellent floating point capabilities of the PA7100, there was no need or motivation for one of ordinary skill in the art to look for and incorporate some other floating point processing unit (such as the one disclosed by Toshiba) in the PA7100LC, even if the peak performance of the Toshiba FPU exceeded the peak performance of the PA7100LC." (emphasis unchanged)

This argument is also not persuasive because patent owner is arguing what might or might not have been obvious to Knebel and Lee, at the time of Knebel and Lee's invention. However, the legal requirement is what would have been obvious at the time of patent owner's invention, several years in the future from Knebel and Lee's invention. At that later time, the general level of knowledge in the art evidences that one of skill would have recognized that even higher floating point performance was becoming very desirable [4] Accordingly, at the time of patent owner's invention, it would have been obvious to one of skill in the art to provide a newer, upgraded, system with higher floating point performance, and one of skill in the art would have therefore been motivated to add a system such as Toshiba to the

4 See for example the document authored by Linley Gwennap entitled "Digital, MIPS Add Multimedia Extensions" published November 18, 1996 where on pg. 24, col. 2, in the section entitled "MIPS V Boosts FP Performance the author describes that the MIPS designers disclose that increasing floating point performance is useful for "many applications, incluing 3D graphics and signal processing".

system of Knebel and Lee in order to obtain the enhanced floating point performance that Toshiba offered.

46. In the remarks at pg. 53, patent owner asserts:

> That: "As previously discussed, claim 18 requires more than just partitioning of the data, it requires partitioning of the data that is dynamic to account for the elemental width of the data. As previously discussed with respect to the anticipation rejection of claim 18 based upon Toshiba, this limitation of claim 18 is not disclosed by Toshiba. Patent owner submits that this deficiency of Toshiba is not cured either by Knebel or Lee."

This argument has already been treated above beginning on pg. 22.

47. In the remarks at pg. 53, patent owner asserts:

> That: "As previously discussed, the 'dynamic partitioning' claim language requires more than just partitioning of the data, it requires partitioning of the data that is dynamic to account for the elemental width of the data. Such dynamic partitioning corresponds to the ability to partition the data one way for an instruction, then partition data another way for the immediately subsequent instruction, to account for a different size of the data field. Such a capability of dynamically partitioning data between successive instructions is not provided by the PA7100LC as disclosed by Knebel and Lee."

As was pointed out in the previous response, this feature is taught by Toshiba as explained previously beginning on pg. 22. Accordingly, as Toshiba has already disclosed this feature, the references to Knebel and Lee have no requirement to additionally disclose the same feature.

Rejection of claim 42 and 46 in view of the Knebel/HP7100LC article and the ILLIAC IV Programming Manual (¶ 173) - Maintained

48. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claims 40-42 in view of Knebel/HP7100LC and the Watkins/Sun article (¶ 176) - Maintained

49. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claim 45 in view of Knebel/HP7100LC, Ide/Toshiba, and Tullsen/Multithreading (¶ 178) - Maintained

50. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claim 41 in view of ILLIAC IV and Watkins/Sun (¶ 189) - Withdrawn

51. Patent owner's arguments against the teachings of the ILLIAC IV reference

were convincing that the ILLIAC IV reference does not teach aspects of claim 18. Accordingly, the ILLIAC IV reference also does not disclose claim 41 and therefore the rejection of claim 41 in view of ILLIAC IV and Watkins/Sun is withdrawn.

Rejection of claims 40-42 in view of Spaderna/Sharp and Watkins/Sun (¶ 208) - Maintained

52. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claim 45 in view of Spaderna/Sharp and the Tullsen/Multithreading article (¶ 214) - Maintained

53. As patent owner has provided no details "which distinctly and specifically point out the supposed errors in the examiner's action" and no details "pointing out the specific distinctions believed to render the claims ... patentable over [the] applied references" (37 CFR § 1.111(b)) the rejection is maintained.

Rejection of claims 18, 27-29, 31-33, and 46 in view of Kimura/Fujitsu and Fujitsu '820 application (¶ 216) - Withdrawn

54. In the remarks at pg. 55, patent owner asserts:

> That: "[the] Third Party Requester is misinterpreting the language of Kimura. In the section referenced by the Requester, Kimura states that

'For the GMICRO family to have original architecture, it is very important to thoroughly plan the product line and software assets. The six companies Hitachi Manufacturing, Mitsubishi Electronics, Oki Electronic Industries, Matsushita Electrical Production, Toshiba, and Fujitsu are planning to unify specifications and share development.'

See Kimura at pg. 90 second column paragraph before section 2.2.

This paragraph merely indicates that Fujitsu is planning to unify specifications and share development. Patent Owner respectfully submits that this does not provide any motivation to combine Kimura with Fujitsu '820."

55. Patent owner's remarks above regarding the third party requester's assertion of obviousness is found convincing. The mere fact that Fujitsu may have been planning to unify specifications and share development does not provide sufficient motivation to specifically combine Kimura with Fujitsu '820. Therefore, the above rejection is withdrawn.

Rejection of claim 45 in view of AltiVec and the Tullsen/Multithreading article (¶ 225) - Withdrawn

56. Patent owner's arguments in favor of their priority claim has resulted in a withdrawal of the finding of lack of continuity to the parent application presented in the previous office action. As a result, rejections based upon intervening references, such as Tyler/AltiVec and the AltiVec Manual are withdrawn as not having a publication date sufficient to qualify as valid prior art against the claims.

Rejection of claims 30 and 47 in view of AltiVec and Fukaya/Hitachi (¶ 227) - Withdrawn

57. Patent owner's arguments in favor of their priority claim has resulted in a

withdrawal of the finding of lack of continuity to the parent application presented in the previous office action. As a result, rejections based upon intervening references, such as Tyler/AltiVec and the AltiVec Manual are withdrawn as not having a publication date sufficient to qualify as valid prior art against the claims.

58. In the remarks at pg. 58-59, patent owner asserts:

> That: "The PTO must consider "all rebuttal arguments and evidence," including "secondary considerations" of nonobviousness such as commercial success, skepticism by others, proceeding contrary to conventional wisdom, praise by others, and copying. ...
>
> Attached are the declarations of John Moussouris, a co-inventor of the '765 Patent and CEO of MicroUnity ("the Moussouris Declaration"), and Ronald S. Alepin, an expert in the computer industry ("the Alepin Declaration"). ...
>
> Substantial weight is properly accorded to evidence of nonobviousness when the proponent "establish[es] a nexus between the rebuttal evidence and the claimed invention." MPEP 2144.08. Here, the Moussouris and Alepin Declarations and their accompanying exhibits reflect a concrete nexus exists between the claimed inventions in the '765 Patent and these secondary indicia of nonobviousness."

Patent owner's submitted declarations will be treated separately below.

Declaration of Ronald S. Alepin

Patent owner is reminded of the nexus requirement as stated in MPEP 716.01 (b):

> Nexus Requirement and Evidence of Nonobviousness
>
> TO BE OF PROBATIVE VALUE, ANY SECONDARY EVIDENCE MUST BE RELATED TO THE CLAIMED INVENTION (NEXUS REQUIRED)
>
> The weight attached to evidence of secondary considerations by the examiner will depend upon its relevance to the issue of obviousness and the amount and nature of the evidence. Note the great reliance apparently placed on this type of evidence by the Supreme Court in upholding the patent in United States v. Adams, 383 U.S. 39,148 USPQ 479 (1966). To be given substantial weight in the determination of obviousness or nonobviousness, evidence of secondary considerations must be relevant to the subject matter as claimed, and therefore the examiner must determine whether there is a nexus between the merits of the claimed invention and the evidence of secondary considerations.

> Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 305 n.42, 227 USPQ 657, 673-674 n. 42 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986). The term "nexus" designates a factually and legally sufficient connection between the objective evidence of nonobviousness and the claimed invention so that the evidence is of probative value in the determination of nonobviousness. Demaco Corp. v. F. Von Langsdorff Licensing Ltd., 851 F.2d 1387, 7 USPQ2d 1222 (Fed. Cir.), cert. denied, 488 U.S. 956 (1988).

And in MPEP 2144.08:

> However, to be entitled to substantial weight, the applicant should establish a nexus between the rebuttal evidence and the claimed invention, i.e., objective evidence of nonobviousness must be attributable to the claimed invention. The Federal Circuit has acknowledged that applicant bears the burden of establishing nexus, stating:
>
> > In the ex parte process of examining a patent application, however, the PTO lacks the means or resources to gather evidence which supports or refutes the applicant's assertion that the sales constitute commercial success. C.f. Ex parte Remark, 15 USPQ2d 1498, 1503 ([BPAI] 1990) (evidentiary routine of shifting burdens in civil proceedings inappropriate in ex parte prosecution proceedings because examiner has no available means for adducing evidence). Consequently, the PTO must rely upon the applicant to provide hard evidence of commercial success.

In the case of the Alepin declaration, the submitted document is expert opinion testimony submitted in the case *MicroUnity Systems Engineering, Inc. v. Dell, Inc.*, Civil Action No. 2-04CV-120 pending in the Eastern District of Texas. The submitted document sets forth no nexus to the ***claimed*** invention in the present patent. In fact, the entire document does not ever mention the ***claimed*** invention in the present patent. It is impossible to establish a nexus between the opinions expressed by the expert opinion document and the ***claimed*** invention in the present patent when the expert opinion document makes absolutely no mention of the ***claimed*** invention. Therefore, having established no nexus to the ***claimed*** invention, the Alepin declaration is not entitled to any significant weight regarding non-obviousness.

The Alepin declaration additionally states that it answers this question:

> "What industry, market and technical factors present in 1999 would influence Intel in hypothetical licensing negotiations for the rights to practice the inventions in the MicroUnity patents at issue in this case?"

It is completely unclear how Mr. Alepin's opinions as to the answers to this question relate to the obviousness of the ***claimed*** invention. Nor does the declaration and patent owner's response clarify how this question is related to the obviousness of the ***claimed*** invention in view of the cited prior art.

Furthermore, the Alepin declaration is simply opinion testimony, a fact expressed by Mr. Alepin in paragraph 4:

> "This report sets forth my opinions on this question and the bases upon which it relies."

Patent owner is reminded that opinion testimony is generally of limited value:

> For example, declarations in which conclusions are set forth without establishing a nexus between those conclusions and the supporting evidence, or which merely express opinions, may be of limited probative value with regard to rebutting a prima facie case. In re Grunwell, 609 F.2d 486, 203 USPQ 1055 (CCPA 1979); In re Buchner, 929 F.2d 660, 18 USPQ2d 1331 (Fed. Cir. 1991). See MPEP § 716.01 (a) through § 716.01(c). MPEP § 2107.02.
>
> Although factual evidence is preferable to opinion testimony, such testimony is entitled to consideration and some weight so long as the opinion is not on the ultimate legal conclusion at issue. While an opinion as to a legal conclusion is not entitled to any weight, the underlying basis for the opinion may be persuasive. In re Chilowsky, 306 F.2d 908, 134 USPQ 515 (CCPA 1962) (expert opinion that an application meets the requirements of 35 U.S.C. 112 is not entitled to any weight; however, facts supporting a basis for deciding that the specification complies with 35 U.S.C. 112 are entitled to some weight);
>
> In assessing the probative value of an expert opinion, the examiner must consider the nature of the matter sought to be established, the strength of any opposing evidence, the interest of the expert in the outcome of the case, and the presence or absence of factual support for the expert's opinion. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986).
>
> Ex parte Gray, 10 USPQ2d 1922 (Bd. Pat. App. & Inter. 1989)

> (statement in publication dismissing the "preliminary identification of a human b-NGF-like molecule" in the prior art, even if considered to be an expert opinion, was inadequate to overcome the rejection based on that prior art because there was no factual evidence supporting the statement);
>
> In re Beattie, 974 F.2d 1309, 24 USPQ2d 1040 (Fed. Cir. 1992) (declarations of seven persons skilled in the art offering opinion evidence praising the merits of the claimed invention were found to have little value because of a lack of factual support);
>
> Although an affidavit or declaration which states only conclusions may have some probative value, such an affidavit or declaration may have little weight when considered in light of all the evidence of record in the application. In re Brandstadter, 484 F.2d 1395, 179 USPQ 286 (CCPA 1973). (MPEP 716.01(c)(III))

Additionally, for this further reason, the declaration being merely opinion testimony, the Alepin declaration is given little probative weight. Furthermore, the bases for Mr. Alepin's opinions, where they are presented, do not create nor explain any nexus to the ***claimed*** invention, nor do they attribute any additional secondary considerations to the ***claimed*** invention.

Declaration of John Moussouris

59. MPEP § 716.01(c)(III) contains the following quotation:

> In assessing the probative value of an expert opinion, the examiner must consider the nature of the matter sought to be established, the strength of any opposing evidence, the interest of the expert in the outcome of the case, and the presence or absence of factual support for the expert's opinion. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986). (MPEP 716.01(c)(III))

In the case of the declaration of John Moussouris, paragraph 2 of the declaration contains the following statement:

> "2. I am a co-inventor of United States Patent No. 6,643,765 ("the '765 Patent") and the CEO and principal shareholder of MicroUnity Systems Engineering, Inc. ("MicroUnity"), the assignee of the '765 Patent."

Accordingly, as seen from the declaration, Mr. Moussouris is both a co-inventor as well as principal shareholder in the assignee of the '765 patent. This means that Mr. Moussouris has an extreme interest "in the outcome of the case" both by being a named inventor as well as by having a significant financial stake in the outcome of the case. Accordingly, Mr. Moussouris must support his assertions in the declaration with significant factual bases in order to overcome this significant inherent interest on his part in the outcome of this reexamination of the '765 patent.

Nexus between invention and secondary considerations

60. Paragraphs 8-13 of the declaration present a brief summary of the claim language. Because a summary of the claim language alone presents no nexus between that language and the secondary considerations, paragraphs 8-13 alone do not present any showing of a nexus between the ***claimed*** invention and the evidence of secondary considerations.

61. Paragraph 14 indicates that Mr. Moussouris does not have access to Intel's confidential information, but that he is familiar with the publicly available details of Intel's Pentium ® III and Pentium ® 4 processors. This paragraph fails to discuss either the claim language or the evidence. Therefore, this paragraph presents no nexus between the ***claimed*** invention and any of the evidence of secondary considerations.

62. Paragraphs 15-16 present a very brief synopsis of the Intel MMX and SSE implementation. Paragraph 15 asserts a tenuous connection between the Pentium ®

III and Pentium ® 4 processors and claims 11 and 17 generically in that it states that these two processors allow group integer and group data handling as recited in claims 11 and 17. Mr. Moussouris then asserts that in his opinion all Intel products with SSE and/or SSE2 possess all the limitations of the claims, generically:

> "In addition, I believe that all Intel products that include SSE and/or SSE2 possess all of the limitations of at least claims 1, 11, and 17 of the '765 Patent."

This statement by Mr. Moussouris is pure opinion. Mr. Moussouris has presented no evidence that any of the structural hardware features recited in claim 1 are present in the Intel processor design. Mr. Moussouris utilizes the fact that these Intel processors perform group integer and group data handling functions to conclude, without proof, that the hardware structural limitations of the claims are present in the Intel CPU's. However, there are many different manners within which Intel may have implemented these group integer and group data handling functions which different significantly from the recited structure of the claim language. For example, Intel may have implemented their CPU's hardware of the structure to utilize plural individual hardware functional units for each group member instead of implementing the claimed "multi-precision execution unit ... configurable to dynamically partition data". Absent actual proof that Intel's implementation contains the claimed structural features, the opinion of Mr. Moussouris is simply that, his opinion.

> Although factual evidence is preferable to opinion testimony, such testimony is entitled to consideration and some weight so long as the opinion is not on the ultimate legal conclusion at issue. While an opinion as to a legal conclusion is not entitled to any weight, the underlying basis for the opinion may be persuasive. In re Chilowsky, 306 F.2d 908, 134 USPQ 515 (CCPA 1962)
>
> In assessing the probative value of an expert opinion, the examiner must

> consider the nature of the matter sought to be established, the strength of any opposing evidence, the interest of the expert in the outcome of the case, and the presence or absence of factual support for the expert's opinion. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986).

Furthermore, the opinion presented by Mr. Moussouris is directly to the ultimate legal conclusion and as seen from *In re Chilowsky* is by itself not entitled to any weight. Furthermore, the expert presenting the opinion, being both an inventor in the patent at issue and CEO and principal shareholder of MicroUnity, the assignee, has an extremely high interest in the outcome of the case. Accordingly, significant factual support is necessary, and as explained above, paragraph 17 of the declaration fails to provide this required factual support for the presented opinion.

63. Paragraphs 18-23 cite various Intel publications that the declaration argues show significant importance to the SSE and SSE2 instruction set. However, Intel, being both the developer of the technology and publisher of the cited documents would of course present their newest technology in the most positive light possible. No sane developer of a technology would present their new technology in a negative light, even if the negative light were justified. So it is only natural that Intel's own publications would present SSE and SSE2 as a significant technological breakthrough. However, this is not evidence that the remainder of the industry, and that one of ordinary skill in the art, impartial to the technology otherwise, would reach the same conclusion regarding the technology. Additionally, Intel's publications, while painting the technology in a positive light, do not, absent further explanation, provide any nexus connection between the ***claimed*** invention and the

secondary considerations of non-obviousness. As declarant has not provided any further explanation as to how and why these Intel publications present a nexus between the ***claimed*** invention and the secondary evidence, these paragraphs fail to present a nexus in and of themselves.

64. Paragraph 24 argues that a nexus is shown by third party recognition that SSE and SSE2 was a key development in Intel's new CPU's. However, just as explained above, declarant has failed to describe and detail how this recognition is a "factually and legally sufficient connection between the objective evidence ... and the ***claimed*** invention so that the evidence is of probative value ... " *Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 7 USPQ2d 1222 (Fed. Cir.), *cert. denied*, 488 U.S. 956 (1988) (MPEP 716.01(b)). I.e., there is no explanation how this recognition is in any way recognition of the claimed features of the invention. At best, the recognition is merely recognition of the general idea of SSE and SSE2 type operations and that these type operations are useful. But recognition that the idea of SSE and SSE2 operations are useful in a broad sense is not recognition of any of the specific claimed features of the invention. Therefore, paragraph 24 also fails to establish a nexus.

65. Paragraphs 25-26 presents that some authors recognize that SSE allowed handicaps of the x86 architecture to be overcome, or in allowing Intel to keep pace with their rival AMD. However, again, declarant has merely presented statements that authors recognize the importance of SSE/SSE2 without explaining how these

statements provide a nexus between the ***claimed*** invention and the evidence of secondary considerations. Patent owner's claims recite a hardware structure for performing the operations necessary to implement group floating point. The fact that Intel's SSE/SSE2 instructions may or may not be "important" provides no evidence that the underlying hardware that Intel designed to perform their SSE/SSE2 instructions is in any way even remotely similar to the hardware structure features recited in patent owner's claims. Accordingly, absent an explanation of how the importance of SSE/SSE2 generally interrelates to the recited hardware structures of patent owner's claims no nexus is shown.

66. Paragraph 27 presents a comparison between Intel's SSE and SSE2 instruction set and patent owner's disclosed instruction set. However, declarant has compared Intel's SSE/SSE2 with the ***disclosed*** invention ***in the specification***. To show a nexus, declarant must compare with the ***claimed*** invention, not the disclosed invention:

> "TO BE OF PROBATIVE VALUE, ANY SECONDARY EVIDENCE **MUST BE RELATED TO THE CLAIMED INVENTION** (NEXUS REQUIRED)
>
> ... To be given substantial weight in the determination of obviousness or nonobviousness, evidence of secondary considerations **must be relevant** to the subject matter **as claimed**, and therefore the examiner must determine whether there is a nexus between the merits of the **claimed invention** and the evidence of secondary considerations. Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 305 n.42, 227 USPQ 657, 673-674 n. 42 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986). The term "nexus" designates a factually and legally sufficient connection between the objective evidence of nonobviousness and **the claimed invention** so that the evidence is of probative value in the determination of nonobviousness. Demaco Corp. v. F. Von Langsdorff Licensing Ltd., 851 F.2d 1387, 7 USPQ2d 1222 (Fed. Cir.), cert. denied, 488 U.S. 956 (1988)." (MPEP 716.01(b), emphasis added)

In attachment Ex. 12, patent owner has compared that certain assembly

language mnemonics for their invention purportedly map to a particular Intel mnemonic for Intel's SSE/SSE2 instruction set.

However, patent owner's claims do not claim instruction mnemonics, the claims recite a processor containing several internal units, including a "multi-precision execution unit ... configurable to dynamically partition data ... [and] capable of performing group floating-point operations ... in partitioned fields and ... and returning catenated results".

The fact that an Intel mnemonic ADDPS may or may not be equivalent to a MicroUnity GF.ADD.32 mnemonic provides no evidence that the Intel mnemonic relates to the claimed details of the invention, including the multi-precision execution unit.

For example, Intel may not "dynamically partition" or Intel may instead utilize plural units to perform group operations in parallel instead of relying on a single partitioned unit.

Accordingly, as declarant's comparison simply compares mnemonics without reference to any claimed features paragraph 27 fails to establish a clear nexus between the ***claimed*** invention and the evidence of secondary considerations.

67. Paragraph 28 presents the conclusion that the improvement Intel achieved by upgrading MMX technology to SSE technology was based upon the claimed features of the '765 patent. However, paragraph 28 simply makes this conclusory statement without providing any underlying factual basis for reaching this conclusion. There is

no evidence presented that any of the claimed hardware features of the present patent are present in Intel's CPU's. As detailed above, Intel's hardware implementation may have taken a completely separate path to achieving the same programmer level functionality. Absent such evidence, it is impossible to include from the fact that Intel's instruction set contains instructions of similar function that Intel utilized any of the claimed features of this patent to obtain that functionality. Accordingly, paragraph 28 also fails to establish a nexus between the ***claimed*** invention and the evidence.

Evidence of commercial success

68. On pgs. 10-12, the declaration avers commercial success and presents evidence purporting to support this argument of commercial success. Each piece of evidence will be treated in turn below.

69. Paragraph 30 argues that attachment Ex. 13 is evidence of commercial success of the invention. However, Ex. 13 simply shows that Intel provided a positive outlook for their Pentium ® III CPU, which is to be expected. Naturally the creator of a new CPU will sing its praises in any document, in order to attempt to convince a larger group of individuals that they need to adopt this new CPU. However, Ex. 13 does not show any success, commercial or otherwise. The document cites no sales figures, and does not indicate that any supposed "success" was derived from the **claimed** invention. Furthermore, the document itself is actually a future prediction, in that it was predicting that the Internet was believed

to become important, and that Intel believed that their new CPU was suitable to take advantage of this importance. However, by being a prediction of what Intel believed would happen in the future, the document can not and does not provide any evidence that any success actually happened, but merely that Intel believed that the Internet would become important in the future.

70. Paragraph 31 argues that attachment Ex. 14 is evidence of commercial success of the invention. However, for the same reasons outlined above regarding attachment Ex. 13, attachment Ex. 14 also fails to show any success, commercial or otherwise. It cites no sales figures, does not indicate that any supposed "success" was derived from the ***claimed*** invention, and is simply a future prediction of what the opinion of Intel was as to what would become important in the future. Furthermore, the document is simply Intel singing their own praises for their new CPU, which is to be expected from the developer of a new CPU.

71. Paragraph 32 argues that attachment Ex. 15 is evidence of commercial success of the invention. However, for the same reasons outlined above regarding attachment Ex. 13, attachment Ex. 15 also fails to show any success, commercial or otherwise. It cites no sales figures and does not indicate that any supposed "success" was derived from the ***claimed*** invention. The document is simply Intel providing a more technical look at the technology in their new CPU and singing their own praises for this new technology, which is to be expected from the developer of a new CPU.

72. Paragraph 32 additionally argues that attachment Ex. 16 is evidence of commercial success of the invention. However, for the same reasons outlined above regarding attachment Ex. 15, attachment Ex. 16 also fails to show any success, commercial or otherwise. It cites no sales figures and does not indicate that any supposed "success" was derived from the ***claimed*** invention. The document is simply Intel providing a more technical look at the technology in their new CPU and singing their own praises for this new technology, which is to be expected from the developer of a new CPU.

73. Paragraph 33 argues that attachment Ex. 17 is evidence of commercial success of the invention. Patent owner is arguing that because attachment Ex. 17 states "the 'Pentium II is dead.'" that this shows that Intel's new Pentium ® III CPU was a commercial success. However, patent owner is actually reading the statement totally out of context and attempting to attach to it a meaning wholly different from the meaning the document itself attaches. Pertinent contextual quotations from the document appear below:

> "Dell is proclaiming the death of Intel's Pentium II processor while it sings the praises of the low-cost Celeron chip"
>
> "Carl Everett, senior vice president in charge of personal systems at Dell says there is such a small delta between the two chips [Pentium II & Celeron] that it's demise [Pentium II] is a foregone conclusion. 'You only have a two to four percent difference in performance between Pentium II and the Celeron. It's very nominal,"
>
> Paul Otellini, general manager of the Intel Architecture Group, has said that phasing out the Pentium II fits in with its overall plan for the Celeron chip." (emphasis added)

As seen from the contextual quotations above, when the statement "the Pentium II is dead" is read in its proper context, the death of the Pentium ® II

comes not from the Pentium ® III, but from the Celeron ® chip. So any success shown by attachment Ex. 17 would be a success of the Celeron ® chip, not success of the Pentium ® III chip. Any success shown for the Celeron ® is immaterial to the Pentium ® III chip, which is the chip that patent owner argues contains their ***claimed*** invention.

74. Paragraph 32 additionally argues that attachment Ex. 18 is evidence of commercial success of the invention. However, the attachment merely states that Intel had announced the phasing out of the Pentium II CPU. Declarant has presented no evidence that this phasing out of the Pentium II CPU was in any way the result of any supposed success of the Pentium ® III CPU. Furthermore, when weighed against the statement of Mr. Paul Otellini quoted above from attachment Ex. 17 that phasing out the Pentium ® II fits with Intel's overall plans for the Celeron ® chip, attachment Ex. 18 can not be seen as indicating that the Pentium ® II was being phased out because of the Pentium III ® CPU, but was instead phased out due to the Celeron ® chip. Patent owner has presented no evidence that this phase out was in any way the direct result of the **claimed** invention features. Accordingly, the attachment carries little convincing weight.

75. Paragraph 34 argues that attachment Ex. 19 is evidence of commercial success of the invention. Attachment Ex. 19 is Intel's 10-K SEC filing for the 2004 year. Patent owner simply argues that because the microprocessor revenue accounted for well over half of Intel's overall revenue that this is evidence of

commercial success. Patent owner is reminded of the requirements for sales figures to show commercial success:

> Gross sales figures do not show commercial success absent evidence as to market share, *Cable Electric Products, Inc. v. Genmark, Inc.*, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985), or as to the time period during which the product was sold, or as to what sales would normally be expected in the market, *Ex parte Standish*, 10 USPQ2d 1454 (Bd. Pat. App. & Inter. 1988). (MPEP § 716.03)

The sales figures supplied by patent owner at best show only gross sales. Absent from the evidence is material showing market share and material showing what sales would normally be expected in the market. Patent owner has failed to show that any increased sales were the direct and immediate result of the ***claimed*** invention. Absent any nexus between the cited sales figures and the ***claimed*** invention, the document carries little probative weight.

76. Paragraph 33 argues that attachment Ex. 20 is evidence of commercial success of the invention. However, Ex. 20 is again a document that is giving a future prediction of what the author's opinion are of things to come. The article indicates that it was believed at the time of publication that multimedia capabilities would be important. However, Ex. 20 provides no evidence that such argued successes did actually occur. Any success which might be seen from the text of Ex. 20 is insufficient given that patent owner has not shown that any success was derived directly from the ***claimed*** invention:

> In considering evidence of commercial success, care should be taken to determine that the commercial success alleged is directly derived from the invention claimed, in a marketplace where the consumer is free to choose on the basis of objective principles, and that such success is not the result of heavy promotion or advertising, shift in advertising, consumption by purchasers normally tied to applicant or assignee, or other business events

> extraneous to the merits of the claimed invention, etc. In re Mageli, 470 F.2d 1380, 176 USPQ 305 (CCPA 1973) (MPEP 716.03)

Furthermore, attachment Ex. 20 does not indicate that any success of any form occurred. This stems directly from the fact that Ex. 20 is a future predicting article. Without hard evidence that success occurred, the document shows little evidentary weight.

77. Paragraph 35 additionally argues that attachment Ex. 21 is evidence of commercial success of the invention. Patent owner relies upon one single sentence from Ex. 21: "After Intel's success with the Pentium 4's SSE2 instruction set". Attachment Ex. 21 indicates that Intel may have enjoyed some success, but no sales figures have been provided and no evidence of what expected sales might have been.

> Merely showing that there was commercial success of an article which embodied the invention is not sufficient. Ex parte Remark, 15 USPQ2d 1498, 1502-02 (Bd. Pat. App. & Inter. 1990). (MPEP 716.03)

Evidence of skepticism/counter to conventional wisdom

78. Paragraphs 36-37 argue that experts in the art were skeptical of the MicroUnity system, citing attachment Ex. 22 as evidence showing such skepticism. However, Mr. Moussouris quotes the skepticism out of context and then attempts to attach this out of context skepticism to the invention instead of to the claimed features of the patent. The actual contextual quotes from Ex. 22 are as follows:

> "Skeptics abound. Mr. Moussouris's plan requires daunting software development and breakthroughs in chip-production processes."
>
> "Mr. Moussouris's chips certainly defy conventional chip-industry wisdom. The

> chips' internal clocks will operate at a billion ticks a second, or 10 times the clock speed of Intel's fastest PC chip. Most chip experts didn't expect anybody to reach that clock speed for several years."
>
> "MicroUnity, surprisingly, has more programmers than hardware engineers. That's because media processors require new operating systems and development software."

When the skepticism is viewed in its proper context of the remainder of the article, it is easily seen that the experts were skeptical as to whether MicroUnity could produce the necessary software (i.e., new operating systems and development software), skeptical as to whether MicroUnity could create the breakthrough chip-production processes (silicon chip integration and fabrication technology), and skeptical that MicroUnity could achieve the claimed clock speeds ("Most chip experts didn't expect anybody to reach that clock speed for several years" Ex. 22). As seen above, the skepticism is related to aspects unrelated to the features of the claims of the patent. There is no evidence that the skepticism extended to a "multi-precision execution unit ... configurable to dynamically partition data ..." as claimed. In fact, the skepticism did not even make any mention of the group floating point operation concept that forms the basis for the claimed hardware features. Accordingly, there is no nexus between the evidence of skepticism and the features of the ***claimed*** invention, and attachment Ex. 22 has little evidentary weight as a result.

Evidence of industry praise and adoption and copying by others

79. Paragraphs 40-41 argue that attachment Ex. 23 is evidence of industry praise. While the document does appear to praise the SSE2 instruction set, the author also states:

> "The majority of content in this article is pure speculation by me, Rick C. Hodgin."

Given that the majority of the document is merely opinion, the content must be weighed against the requirements relating to opinion testimony:

> Although factual evidence is preferable to opinion testimony, such testimony is entitled to consideration and some weight so long as the opinion is not on the ultimate legal conclusion at issue. While an opinion as to a legal conclusion is not entitled to any weight, the underlying basis for the opinion may be persuasive. In re Chilowsky, 306 F.2d 908, 134 USPQ 515 (CCPA 1962) (MPEP 716.01(b))

Attachment Ex. 23 does not provide any underlying basis for the opinions expressed therein, accordingly there is no underlying basis to give any weight. Furthermore, because the opinion expressed is directly related to the legal conclusion at issue, as seen above, it is not entitled to any weight. Accordingly, attachment Ex. 23 has essentially no evidentary weight.

80. Paragraph 42 argues that attachment Ex. 1 praises SSE. The cited section of Ex. 1, section 5.2 Benefits indicates that SSE is a beneficial addition because it allows a reduction in the number of instructions executed to perform a given operation on a given data set. While this at first may appear to be praise, it is in fact simply a statement of a fact that has been known since the dawn of time. Namely that performing some task in parallel using multiple actors will accelerate the completion of that task. Accordingly, document Ex. 1 has little evidentary weight.

81. Paragraph 43 argues that by copying MicroUnity's group floating point operations, that Intel has itself praised the invention. However, merely showing that copying may exist is insufficient:

> Another form of secondary evidence which may be presented by applicants during prosecution of an application, but which is more often presented during litigation, is evidence that competitors in the marketplace are copying the invention instead of using the prior art. However, more than the mere fact of copying is necessary to make that action significant because copying may be attributable to other factors such as a lack of concern for patent property or contempt for the patentees ability to enforce the patent. *Cable Electric Products, Inc. v. Genmark, Inc.*, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). Evidence of copying was persuasive of nonobviousness when an alleged infringer tried for a substantial length of time to design a product or process similar to the claimed invention, but failed and then copied the claimed invention instead. *Dow Chem. Co. v. American Cyanamid Co.*, 837 F.2d 469, 2 USPQ2d 1350 (Fed. Cir. 1987). Alleged copying is not persuasive of nonobviousness when the copy is not identical to the claimed product, and the other manufacturer had not expended great effort to develop its own solution. *Pentec, Inc. v. Graphic Controls Corp.*, 776 F.2d 309, 227 USPQ 766 (Fed. Cir. 1985). See also *Vandenberg v. Dairy Equipment Co.*, 740 F.2d 1560, 1568, 224 USPQ 195, 199 (Fed. Cir. 1984) (evidence of copying not found persuasive of nonobviousness) and *Panduit Corp. v. Dennison Manufacturing Co.*, 774 F.2d 1082, 1098-99, 227 USPQ 337, 348, 349 (Fed. Cir. 1985), vacated on other grounds, 475 U.S. 809, 229 USPQ 478 (1986), on remand, 810 F.2d 1561, 1 USPQ2d 1593 (Fed. Cir. 1987) (evidence of copying found persuasive of nonobviousness where admitted infringer failed to satisfactorily produce a solution after 10 years of effort and expense). (MPEP 716.06)

Patent owner must show two elements to support a secondary consideration of copying. Patent owner must show that Intel copied the ***claimed*** features of the patent, and patent owner must show that Intel attempted and failed for a substantial length of time to independently derive the ***claimed*** features of the patent before resorting to copying the ***claimed*** features. Patent owner has produced no evidence of either necessary part to show copying.

In the first case, patent owner has presented evidence showing that Intel's processor contains instruction mnemonics which represent similar functionality to

patent owner's disclosed invention's instruction mnemonics. However, the fact that Intel added instructions that patent owner purports perform the same **function** as the instructions in patent owner's **specification** is not evidence that Intel copied patent owner's ***claimed*** features. As has been detailed above, Intel's hardware implementation of the structure necessary for performing the **function** of the SSE and SSE2 instruction mnemonics very well may have differed quite substantially from the hardware features ***claimed*** in the instant patent. Patent owner has presented no evidence that the Intel CPU's contain the ***claimed*** structures of the present patent.

Furthermore, in the event that Intel's hardware structure for performing the functions of the SSE/SSE2 mnemonics happened to be identical to patent owner's ***claimed*** invention, patent owner must still present evidence that Intel in fact **copied** patent owner's ***claimed*** features instead of independently inventing the same structure. Patent owner has presented no such evidence of actual copying of patent owner ***claimed*** features by Intel.

In the second case patent owner has also failed to present any evidence that Intel attempted for any substantial length of time of design a similar product but failed and then copied the invention (see *Dow Chem. Co. V. American Cyanamid Co. and Pentec, Inc. v. Graphic Controls Corp. citations above).* In fact, patent owner's attachment Ex. 16 quotation indicates that Intel added the 70 new SSE instructions at only an additional 10% cost in die size. This evidence submitted by patent owner

supports a conclusion that Intel very well may have expended only minimal effort in adding the SSE/SSE2 instruction set to their CPU's.

Accordingly, because patent owner has presented, at best, only evidence that copying of the ***function*** defined by the instructions may have occurred, while failing to present evidence of the necessary additional element for copying (that Intel attempted and failed to design their own solution) and failing to show that Intel copied the ***claimed*** features, the argument in paragraph 43 carries little evidentary weight.

82. Taken as a whole, the fact that the declaration has established a tenuous, minimal nexus at best between the claimed features and evidence of commercial success, and the fact that the evidence does not disclose nor support declarant's arguments as explained above, the declaration and its supporting evidence do not receive sufficient probative weight to outweigh the significant evidence of obviousness presented by the applied references. Accordingly, the declaration is insufficient to overcome the rejections over obviousness.

RESPONSE TIMES ARE SET TO EXPIRE AS FOLLOWS:

For Patent Owner's Response:

TWO (2) MONTH(S) from the mailing date of this action. 37 CFR §1.945. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR § 1.956.

For Third Party Requester's Comments on the Patent Owner Response:

30 DAYS from the date of service of any patent owner's response. 37 CFR

1.947. **NO EXTENSIONS OF TIME ARE PERMITTED.** 35 USC § 314(b)(2).

83. Extensions of time under 37 CFR § 1.136(a) will not be permitted in *inter partes* reexamination proceedings because the provisions of 37 CFR § 1.136 apply only to "an applicant" and not to the patent owner in a reexamination proceeding. Additionally, 35 U.S.C. § 314(c) requires that *inter partes* reexamination proceedings "will be conducted with special dispatch" (37 CFR § 1.937). Patent owner extensions of time in *inter partes* reexamination proceedings are provided for in 37 CFR § 1.956. Extensions of time are not available for third party requester comments, because a comment period of 30 days from service of patent owner's response is set by statute. 35 U.S.C. § 314(b)(3).

84. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be an ActionClosing Prosecution (ACP), will be governed by 37 CFR 1.116, which will be strictly enforced.

85. All correspondence relating to this inter parties reexamination proceeding should be directed:

By Mail to: Mail Stop Inter Parties Reexam
Central Reexamination Unit
Office of Patent Legal Administration
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany St.
Alexandria, VA 22313

86. Any inquiry concerning this communication or earlier communications from the examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

RICHARD L. ELLIS
PRIMARY EXAMINER